STABILITY OF MINIMODULES WITH COPPER PLATED HETEROJUNCTION SOLAR CELLS

Metallization & Interconnection WORKSHOP 2023 for Crystalline Silicon Solar Cells
11TH EDITION

Agata Lachowicz[1], Nicolas Badel[1], Alexis Barrou[1], Vincent Barth[2], Samuel Harrison[2], Nicola Frasson[3], Marco Galiazzo[3], Jun Zhao[1], Bertrand Paviet-Salomon[1], Christophe Ballif[1]
[1] CSEM / [2] CEA INES / [3] AMAT

Neuchâtel, May 9th 2023

OUTLINES

- Process for copper metallization
  on heterojunction solar cells

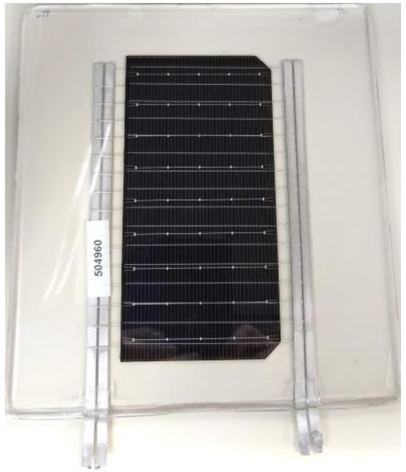
- Minimodules with Smartwire interconnection

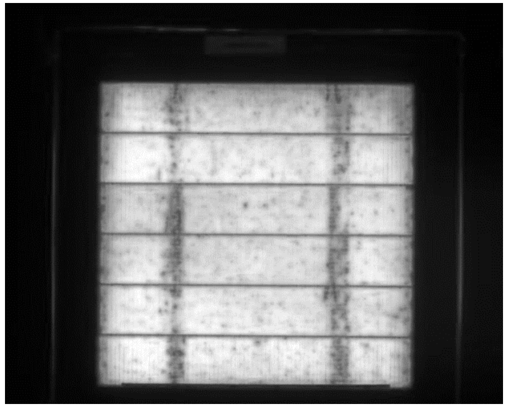
  PTC/DH 3xIEC and PID test results

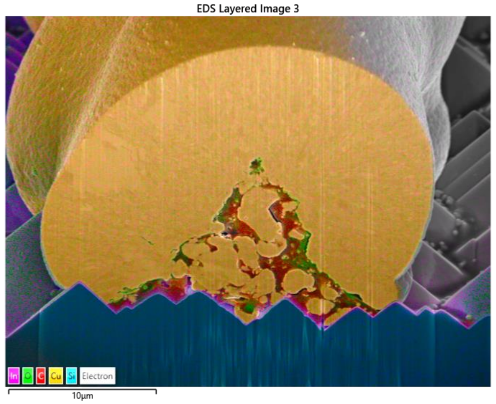
- Shingle modules

  TC 200 / DH 1500h

- Pattern-transfer-printing (PTP) with pure copper paste
  for seed-grid formation





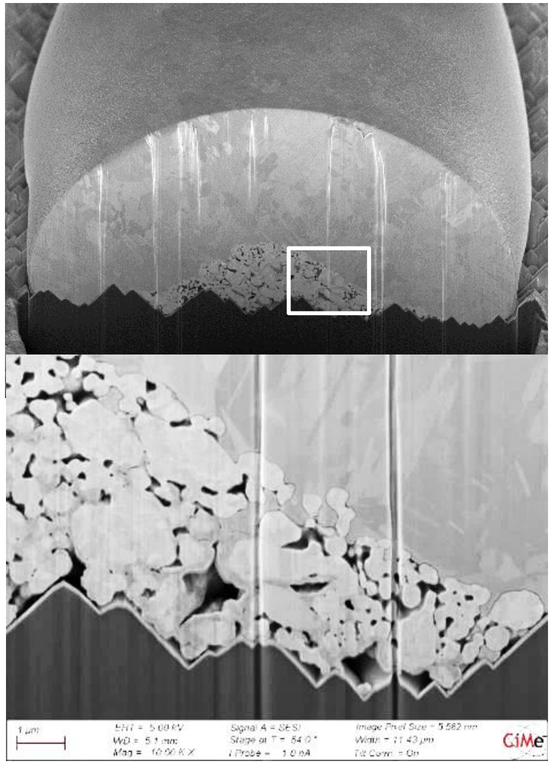


SELF-ALIGNED COPPER ELECTRODEPOSITION PROCESS

- 3-step-process:

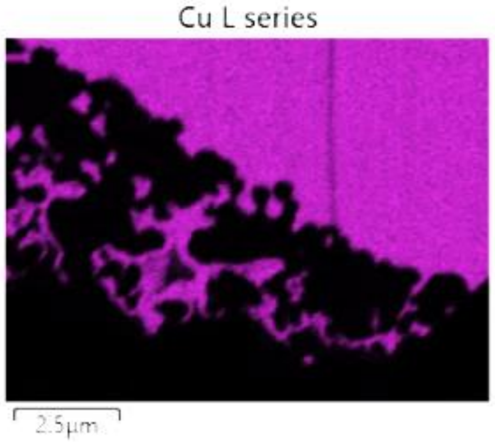
1. • **Seed-grid printing and curing (200°C)**
2. • **Dielectric layer deposition over the entire wafer surface**
3. • **Copper electrodeposition**

- Printing is already part of the production
- A stack of thin ITO and a dielectric layer is one of the strategies followed for Indium reduction [1,2]
- Only plating to add



Cross section: Ag paste, Al_2O_3 masking layer, electrodeposited copper

Copper is deposited also in between paste particles

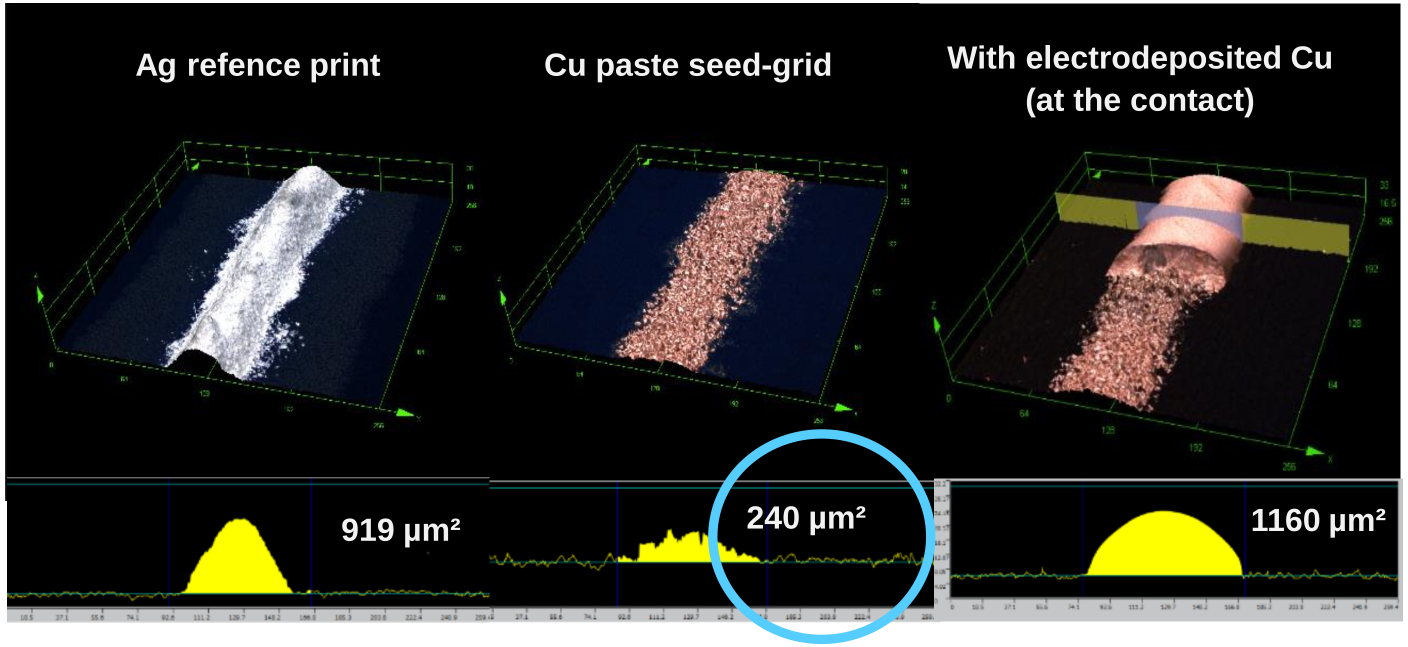


The dielectric layer is not continuous on paste particles ⇨ current for electrodeposition can pass through and copper is deposited selectively on seed-grid positions, whereas TCO area is tightly covered by the dielectric

1 A. Cruz et al., “Optoelectrical analysis of TCO+Silicon oxide double layers”, SOLMAT, 2022
2 S. Janke et al., “Approaches for SHJ cells with low or no In content”, Silicon PV, 2022

csem

COMPARISON LINE RESISTANCE



		Ag ref.	Cu paste	Cu plated
Specific resistivity	**[µΩ·cm]**	**5.3**	**27**	**2.0**
Line resistance per length unit (40 µm screen opening)	**[Ω/cm]**	**1.5**	**95**	**0.3**

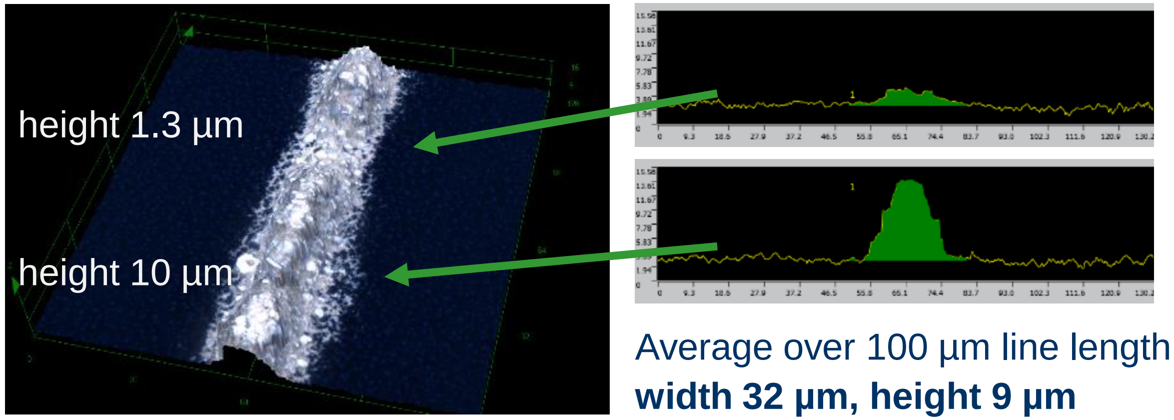
- Pure copper paste can be printed directly on the cell surface since **thin conductive oxides are excellent barriers against copper diffusion** [1,2]
- Electrodeposition is feasible even on thin and resistive lines
  ⇨ low paste laydown for seed-grid formation
- Same efficiency as Ag reference reached with pure Cu paste and electrodeposited Cu on M2 precursors (screen with 40 µm openings). [3]
- Challenging: screen printing of narrow lines without interruptions

1 C. Liu et al., "ITO as Diffusion Barrier Between Si and Cu“, ECS, 2005
2 J. Yu et al., "Tungsten doped indium oxide film", Solmat, 2016
3 A. Lachowicz et al., “Patterning Techniques for Copper Electr.”, Proc. IEEE PVSC, 2021

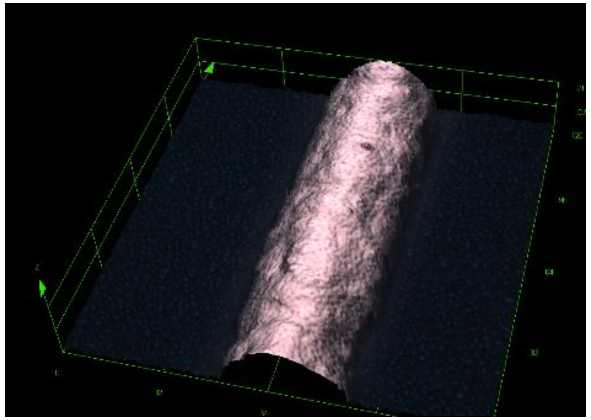
csem

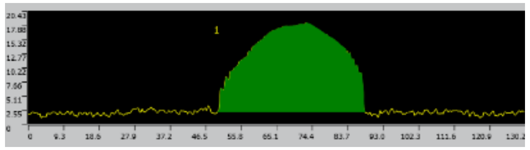
CU ELECTRODEPOSITED ON PRINTED PASTE: SCC

- Copper pastes in development for PV
- **Silver-coated-copper paste (**SCC) used for seed-grid formation, knotless screen



Average over 100 µm line length:
width 32 µm, height 9 µm





Average over 100 µm line length:
width 42 µm, height 16 µm
Levelling effect

Best result so far with SCC paste seed-grid, M6 [1]

M6 industrial HJT precursor	Area [cm²]	Voc [mV]	Jsc [mA/cm²]	FF [%]	Eff [%]
SCC-seed-grid / dielectric layer / electrodeposited copper, 9BB-layout	274.15	742.4	39.9	81.7	24.2

Internal measurement with 9 bars on a gold-chuck, after calibration with a certified M6 cell; cell as plated

1 A. Lachowicz et al., Self-aligned Copper Electrodeposition", Proc. EUPVSEC, 2022

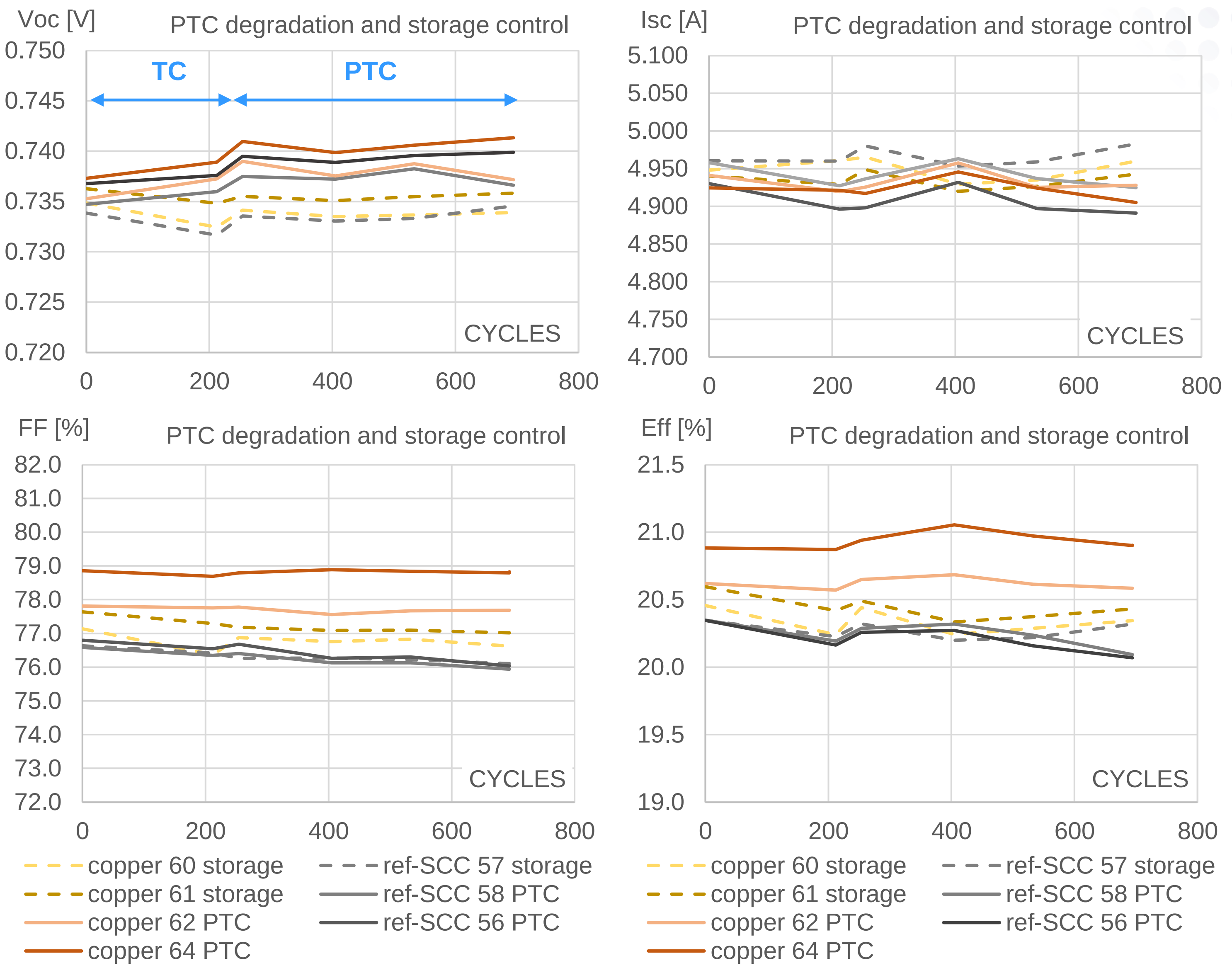
MINIMODULES WITH SMARTWIRE INTERCONNECTION: TC

Storage control: dashed lines - - - - -

SCC-reference.: grey / **dark grey lines**

With copper: orange / **brown lines**

- Reference:
  Silver-coated-copper paste (SCC)
- With copper:
  plated on SCC paste, same paste and same print as the reference, with dielectric layer as plating mask, with capping layer; higher FF
- 1 half-cell, industrial M6 precursors
  Wires: with In-free low melting point alloy and supporting foil
  Polyolefin encapsulant, glass-glass
- **Degradation PTC:**
  SCC-reference: -1.4% after 690 cycles
  With copper: -1.2% storage, -0.2% PTC



MINIMODULES WITH SMARTWIRE INTERCONNECTION: DH

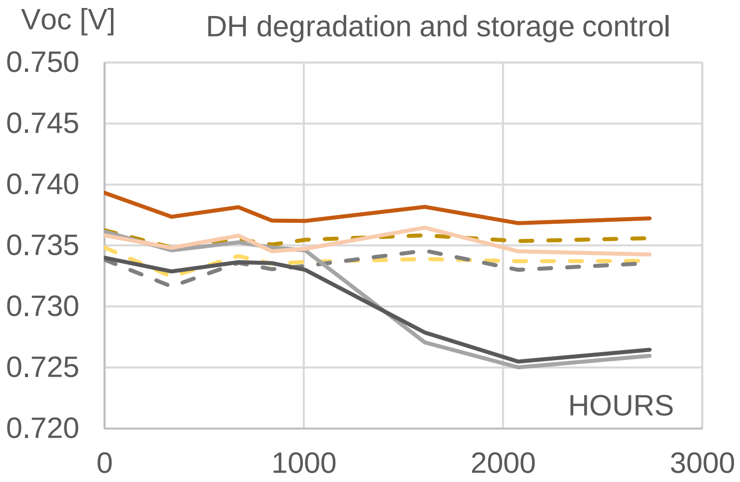
Storage control: dashed lines - - - - -

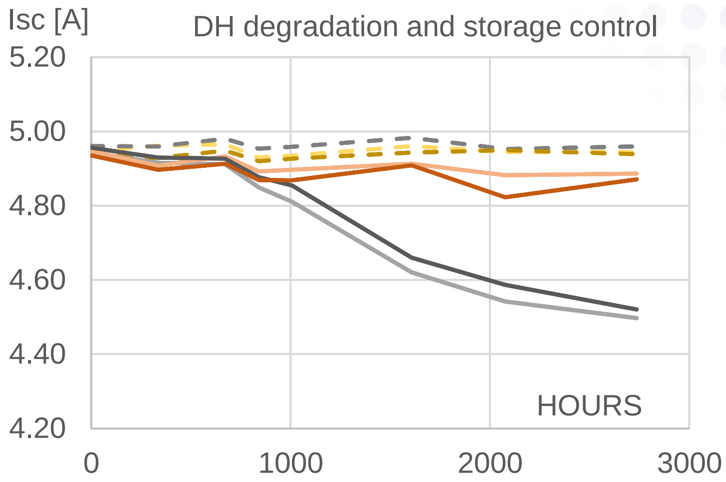
SCC-reference.: grey / **dark grey lines**

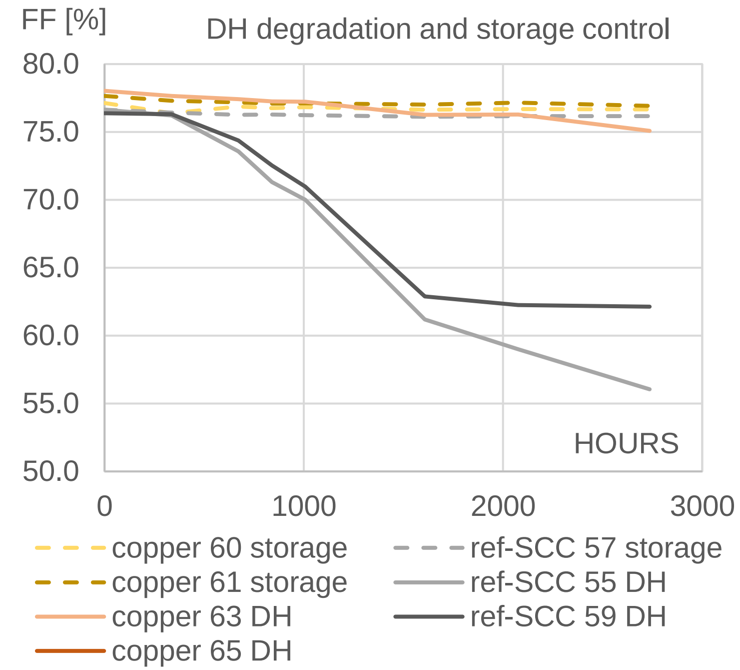
With copper: orange / **brown lines**

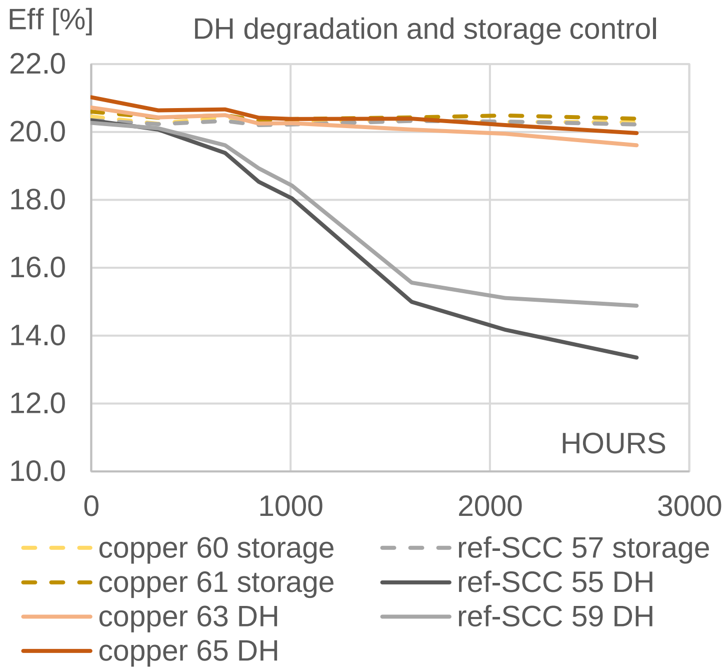
- Strong DH degradation of reference modules with silver-coated-copper paste
  Slight degradation with dielectric layer and plated copper
- In general:
  Good module stability has been proven for SCC paste by the industry, for interconnection with soldered wires as well as for interconnection with Smartwires
- The used paste not previously tested with module materials used in this experiment

- **5% degradation of modules with copper after 2700 h damp-heat**
  To re-test / with another materials







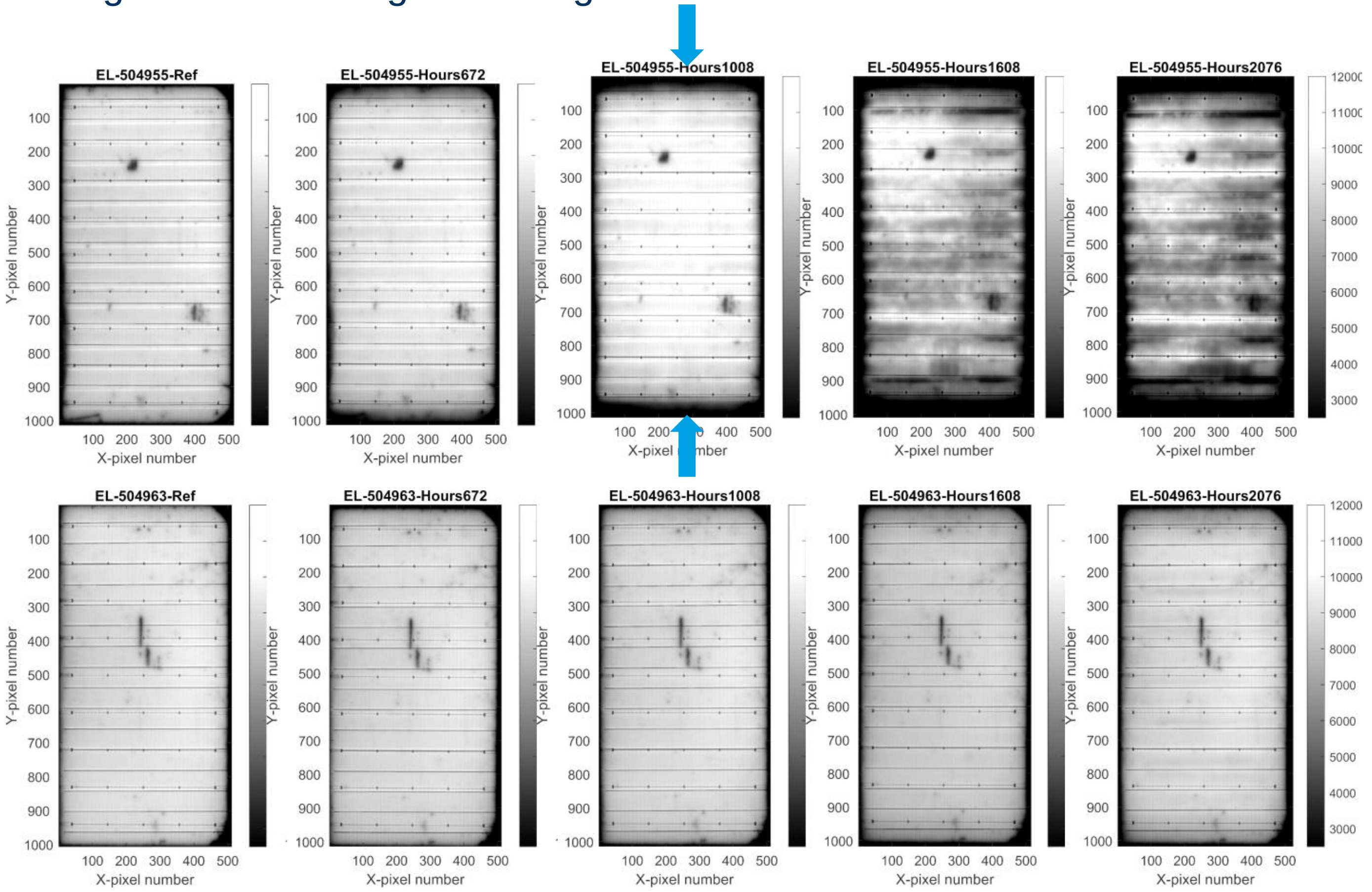


MINIMODULES WITH SMARTWIRE INTERCONNECTION

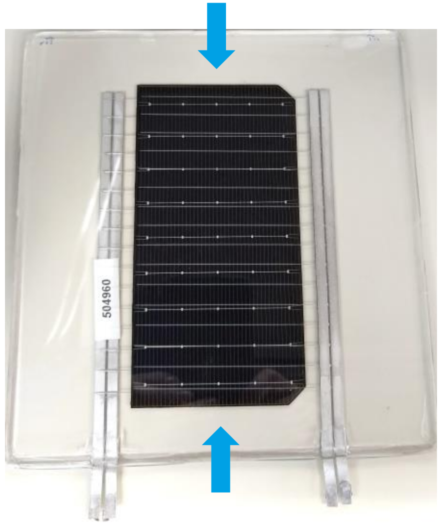
- EL: damp-heat degradation starting at the edges

Seed-grid
SCC paste

SCC paste
+ dielectric layer
+ plated Cu



- 5% degradation of 1-cell-modules with dielectric layer + copper

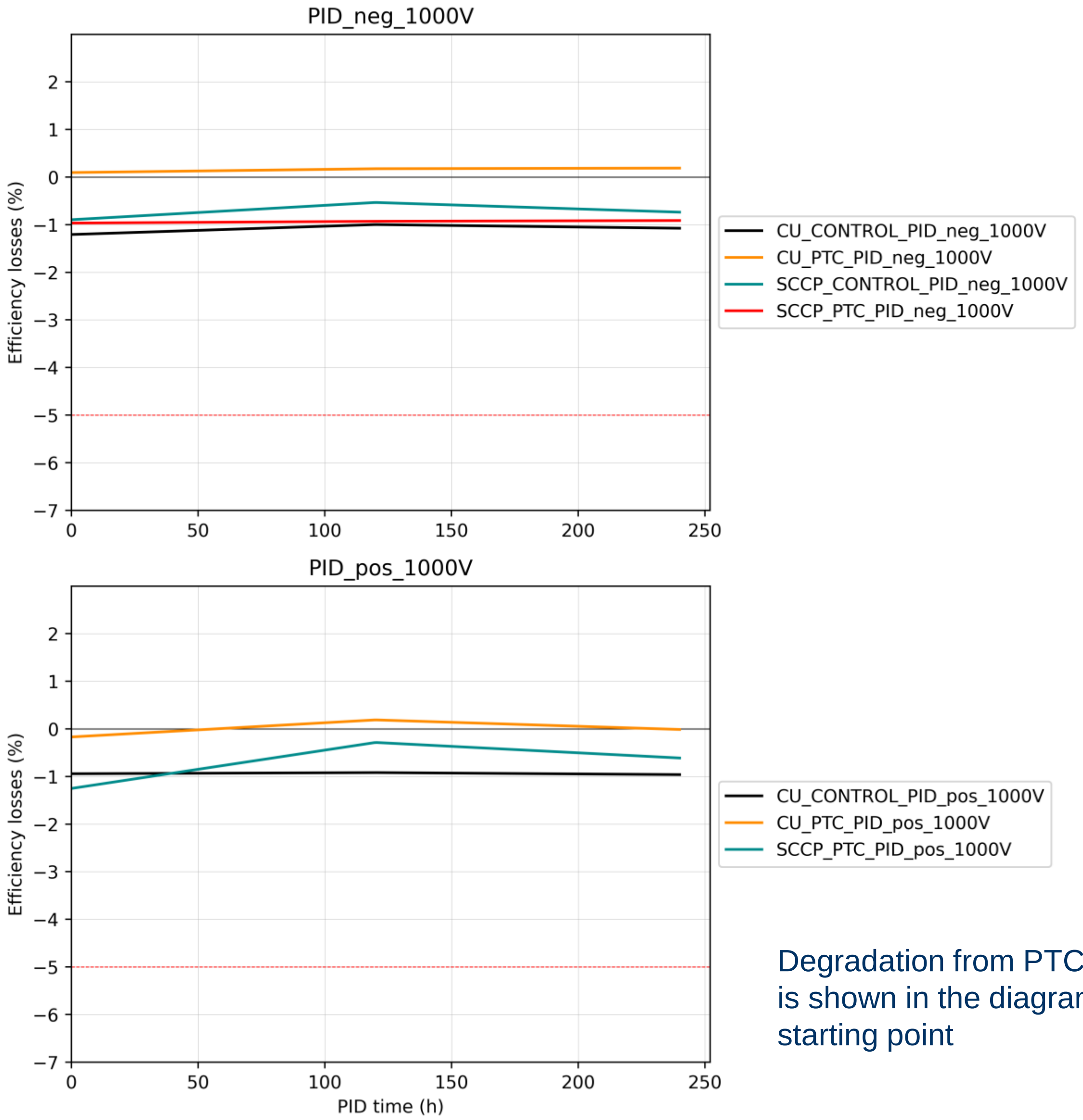


- 1-cell mini-modules: worst case for testing DH degradation? Humidity ingress from (unsealed) module edges close to the cell

MINIMODULES WITH SMARTWIRES: PID

- Modules after storage and PTC have been re-used for PID test
- Conditions:
  85°C/85% rel.H (like DH)
  +1000V or -1000V
  1x IEC norm = 96 h

- **STABLE**
  Tested 2x 96 h



Degradation from PTC or storage is shown in the diagrams as the starting point

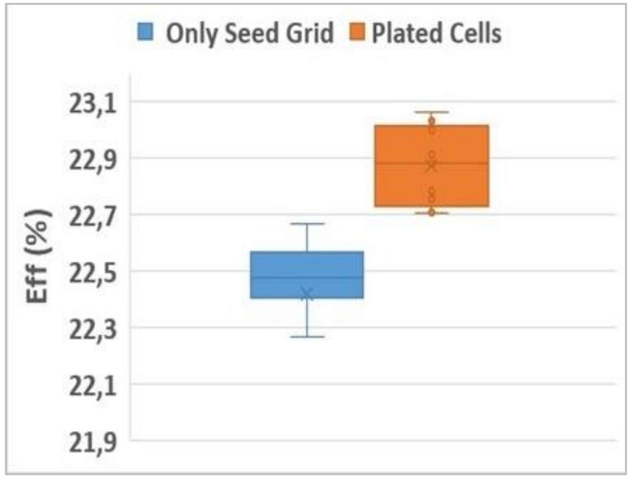
SHINGLE MODULES

- Based on M2 precursors fabricated at CEA INES
  Seed-grid: Ag paste with reduced laydown, single print, lower line aspect ratio
  Layout with 6 shingles and additional pads for contacting for copper electrodeposition

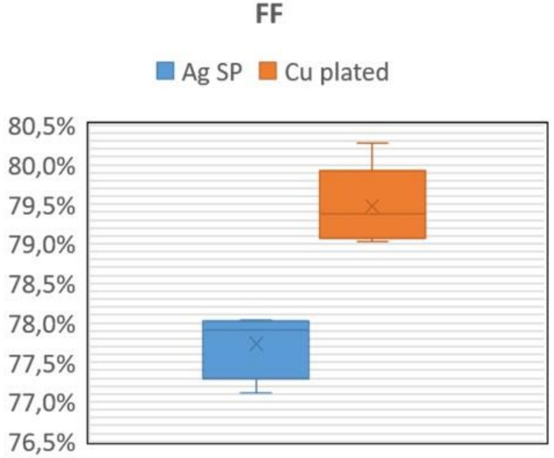
- Plating at CSEM
  Cu thickness ~20 µm

- Shingle separation and stringing on industrial equipment developed by AMAT Italy
  6 shingles, corresponding to 1 M2 cell
  ECA wet deposit per shingle ~3.5 mg

Cells



Modules

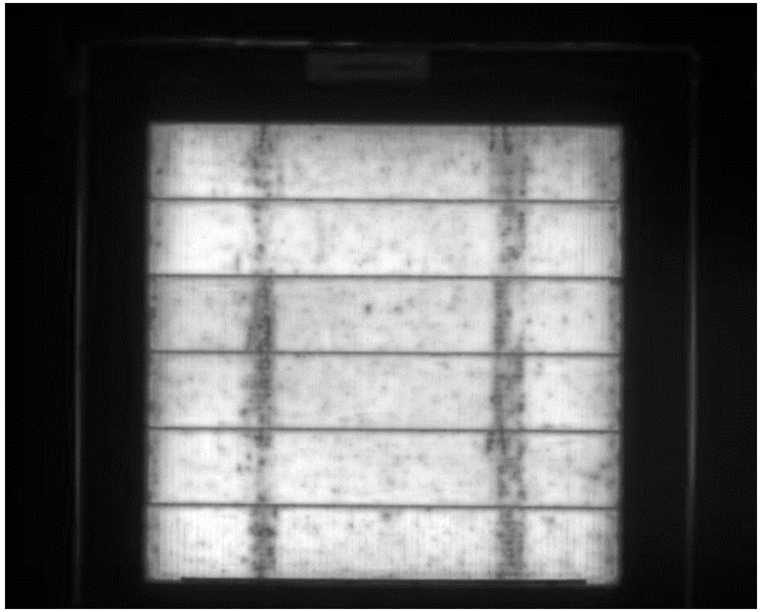


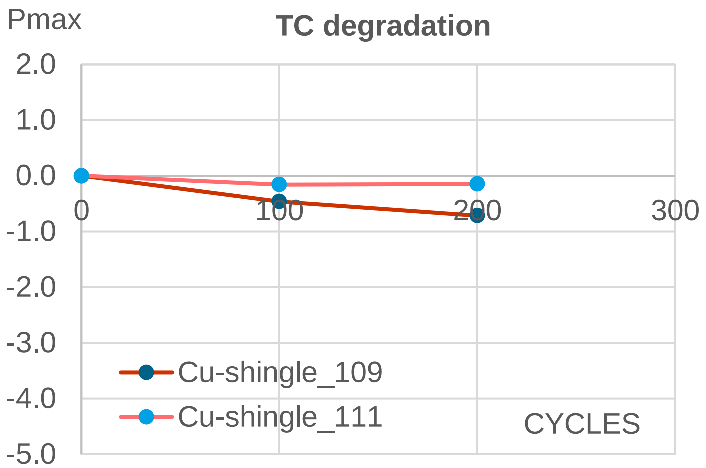
Line resistance	as printed (Ag paste)	w. electrodeposited copper
per shingle width 25 mm	0.43 Ω	0.07 Ω

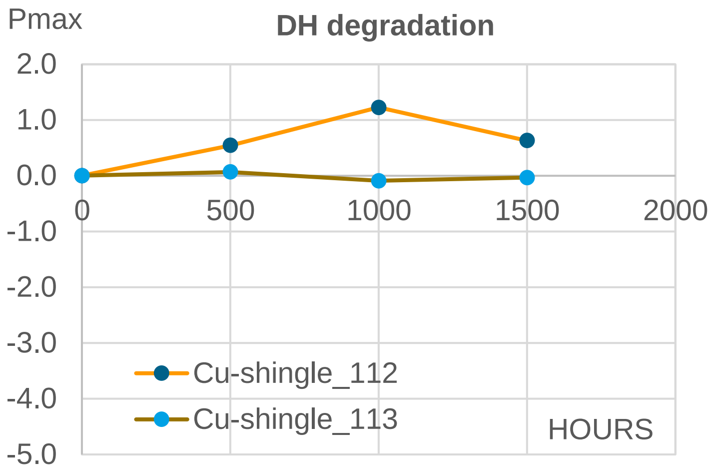
Measurement with Kelvin probes on contacting pads over the width of one shingle tile

SHINGLE MODULES

- Good stability after 200 TC and 1500 h DH, test ongoing





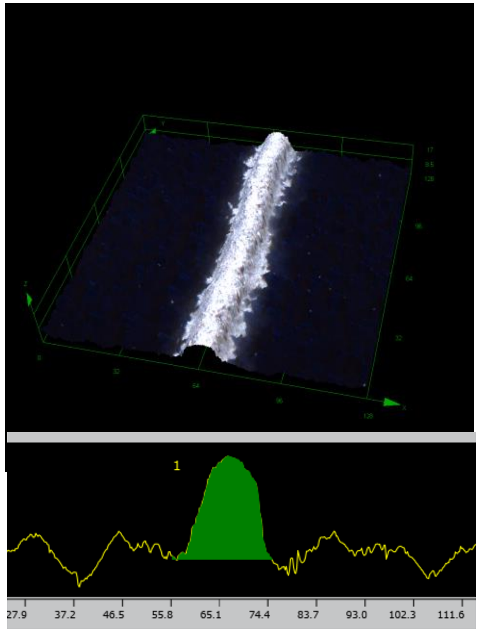


EL module with 6 shingles from M2 cells
Transport belt traces from cell pilot line (vertical)

PATTERN TRANSFER PRINTING FOR SEED-GRID FORMATION

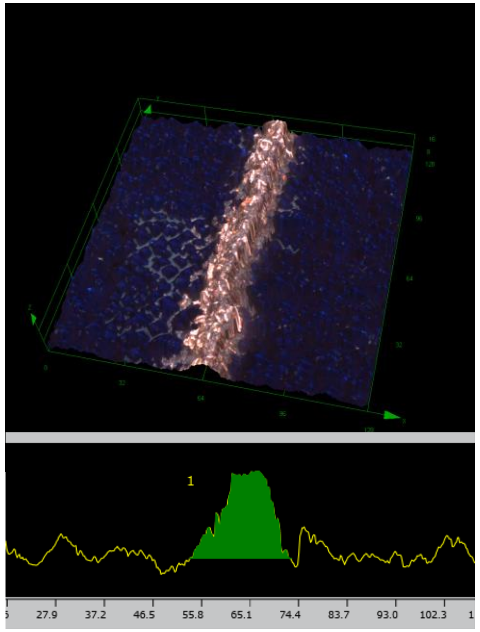
- Goal: narrow copper lines
- Technology developed by DR Utilight – DR Laser. Trenches in a foil are filled with paste. Paste is then transferred to a wafer by laser.
- Uniform line dimensions **No interruptions**
- Comparison resistance contacting pad to contacting pad over 26 mm distance
- Contact resistance measured previously with screen printing: 1.5 mΩ·cm²

Silver-coated copper paste



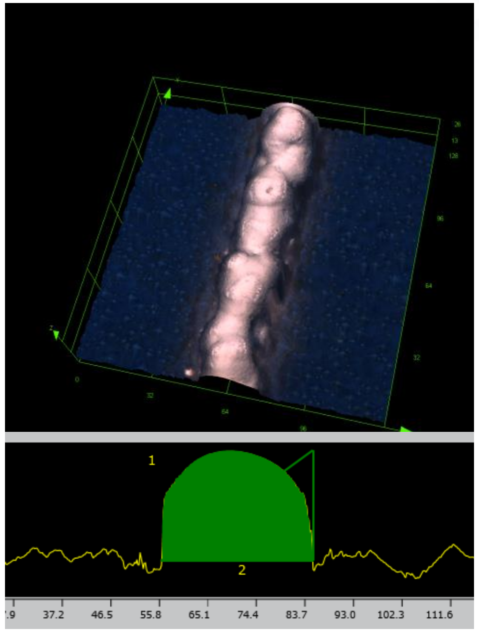
Line width	18.9 µm
Line height	10.3 µm
CS area	116 µm²

Pure copper paste



Line width	21.5 µm
Line height	9.3 µm
CS area	102 µm²

Pure copper paste + electrodeposited copper



Line width	25.0 µm
Line height	17.6 µm
CS area	335 µm²

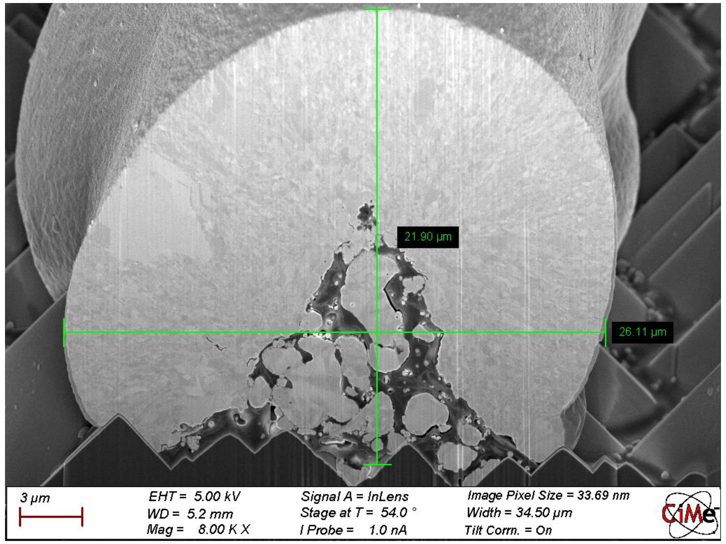
Pad to pad distance 26 mm	SCC paste	Cu paste	Cu paste + electrodeposited Cu
Ω	1.5	5.1	0.18

csem

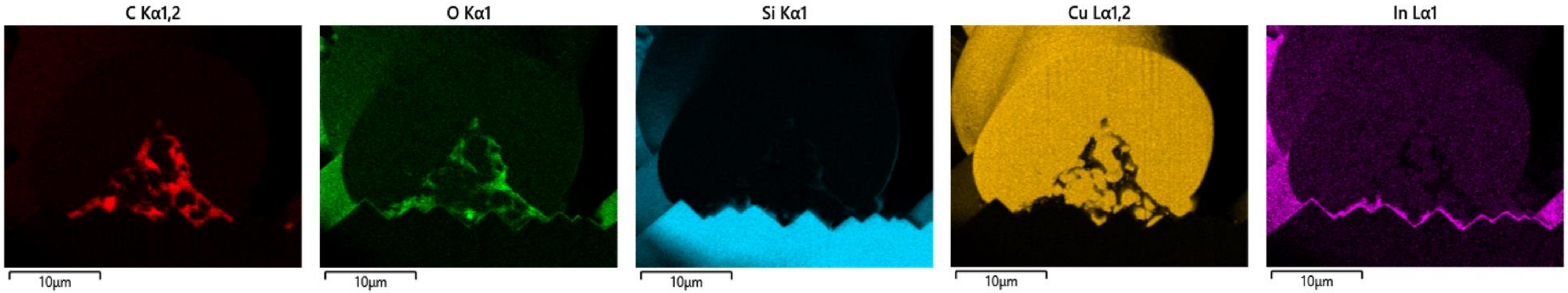
PATTERN TRANSFER PRINTING FOR SEED-GRID FORMATION

- Pure copper paste with micron size copper particles
- Plating mask: dielectric layer
- Copper electrodeposition
- Line width 26.1 µm
  Line height 21.9 µm
- Good adhesion (tape test)

- **Narrow copper lines**



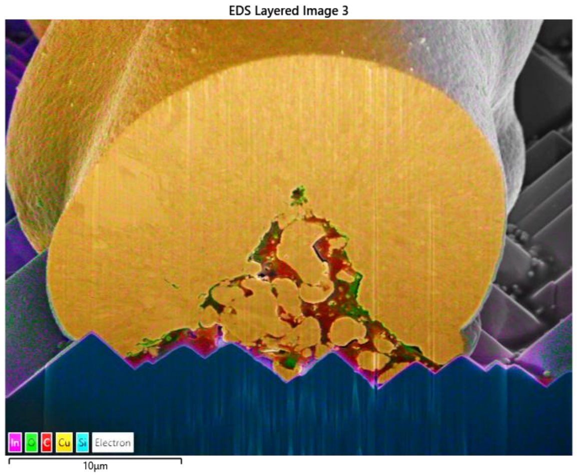
EDX map



SUMMARY AND OUTLOOK

- Module stability with Smartwire interconnection:
  - PTC: very good stability with copper plated metallization ✓
  - PID: very good stability with copper plated metallization ✓
  - DH: -5% after 3xIEC, better stability to prove (with 1-cell and medium size modules)

- In preparation: interconnection with soldered wires
- Ongoing cell experiments: thin ITO and dielectric layer = plating mask For In reduction
- Next: cells with PTP seed-grid for narrow copper lines



Further line width reduction to <20 µm feasible and more triangular shape with conformal plating

csem

THANK YOU VERY MUCH FOR YOUR ATTENTION!

We thank the companies ATOTECH and DUPONT for providing us plating chemistry

We thank the companies DR UTILIGHT and NAMICS for fruitful collaboration

This work has been partially carried out within the European projects HighLite (GA 857793) and Resilex (GA 101058583)

Funded by the European Union

Contact: agata.lachowicz@csem .ch

FACING THE CHALLENGES OF OUR TIME