REDUCTION OF SILVER & INDIUM CONSUMPTION

BY COPPER PLATING WITH A DIELECTRIC MASKING LAYER
FOR SUSTAINABLE PRODUCTION OF HETEROJUNCTION CELLS

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[2] CEA INES, France
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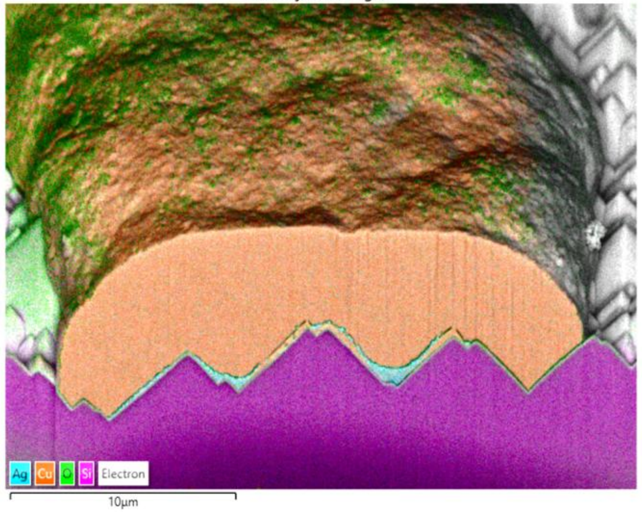
EDS Layered Image 5



Metallization & Interconnection WORKSHOP

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OUTLINES

- PROCESS 3 steps
- CELL RESULTS w. 50 & 30 nm ITO
- DH STABILITY w. copper on 15 nm ITO
- COST & MATERIALS comparison w. SP

- SEED GRID FORMATION BY FLEXTRAIL PRINTING

MATERIALS & COSTS

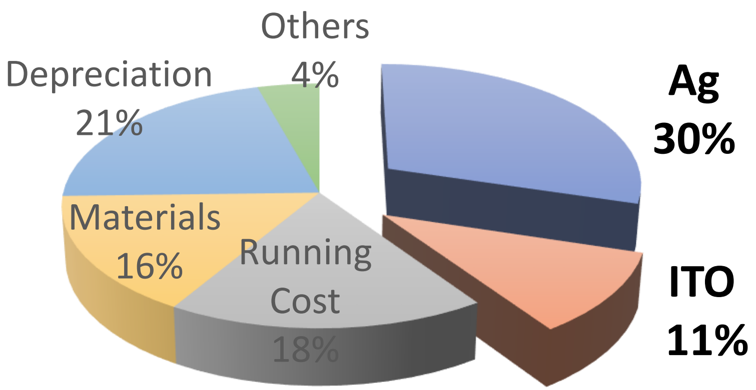
	Current consumption in production	Postulated for SUSTAINABLE TW production [1]
Silver	~10 mg/W *	2 mg/W
Indium	~5 mg/W **	0.38 mg/W

* Depending on layout: with busbars or BB-less

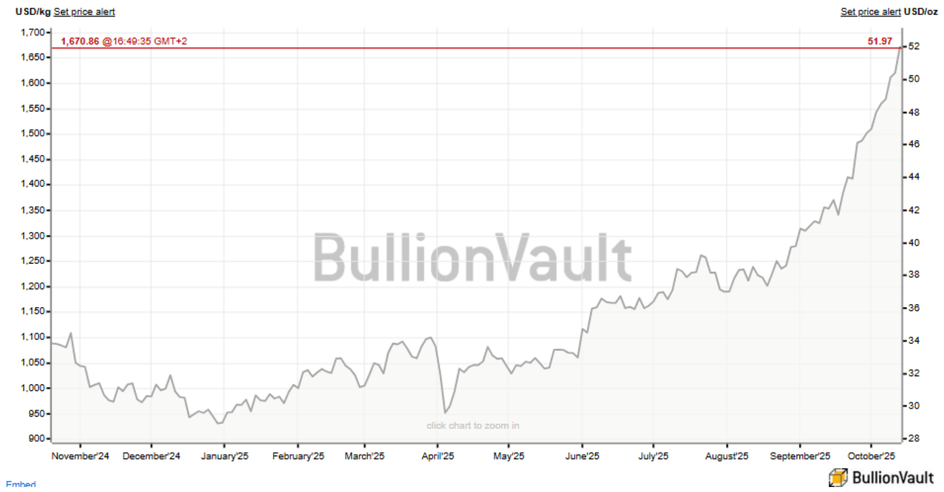
** Calculated Indium amount on a cell with 100 nm ITO on both sides/ ITO-target consumption higher

1 Y. Zhang, M. Kim, W. Li, P. Verlinden and B. Hallam, "Design considerations for multi-terawatt scale manufacturing: challenges and opportunities related to silver, indium and bismutth consumption,“, 2021

Ag & In/ITO: substantial share of cell production cost



Courtesy: Infolink, 2024



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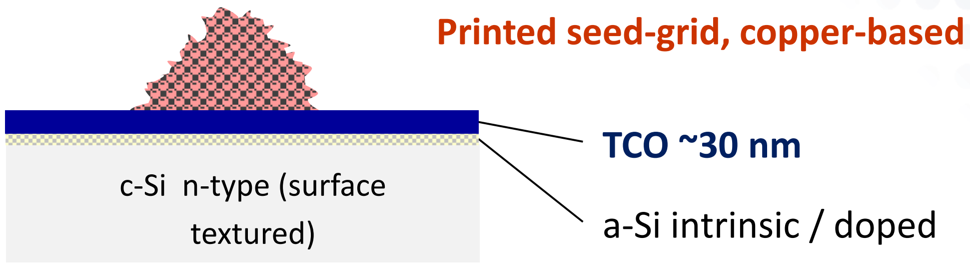
SELF-ALIGNED COPPER ELECTRODEPOSITION

1 • Seed-grid printing on (thin) TCO and curing (200°C)

2 • Dielectric layer deposition over the entire wafer surface

3 • Copper electrodeposition



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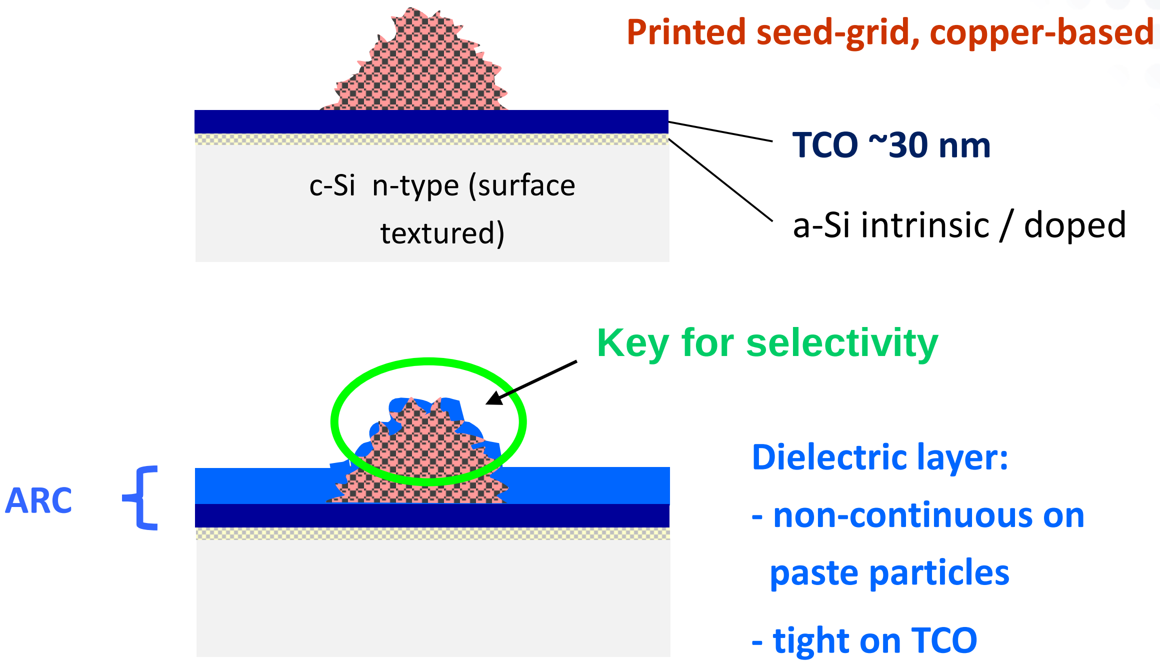

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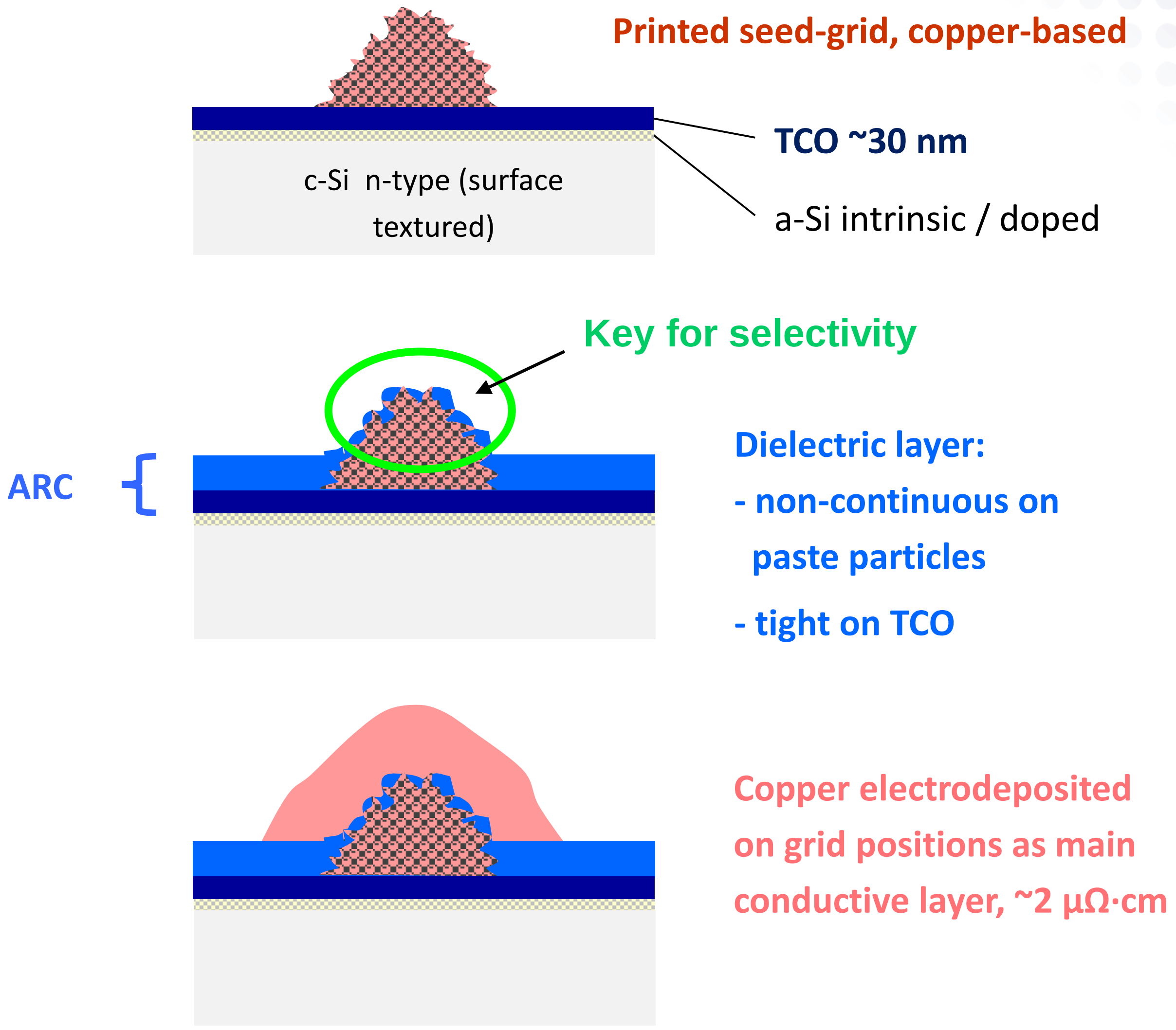

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CELL RESULTS w. 50 nm ITO (1/2 M10)

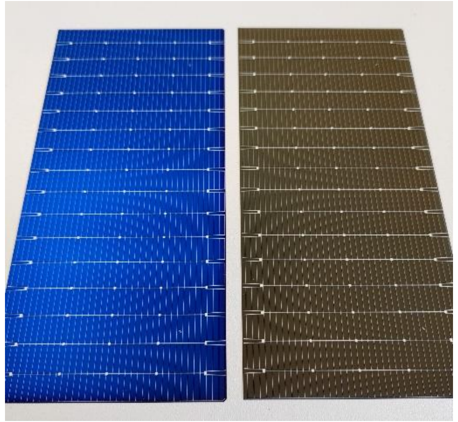
-Customer Sampling A

Group	ITO on the front side	Seed-grid
A ref.	Std. 100 nm	Std. Ag
B	**50 nm**	Narrower openings
C	**50 nm**	Std. Ag
D	**50 nm**	**Ag/Cu**
E	**50 nm**	**On the back: pure Cu paste**

- Precursors from a HJT manufacturer with 50 nm ITO **on the front** and different seed-grid pastes

ITO std. 100 nm

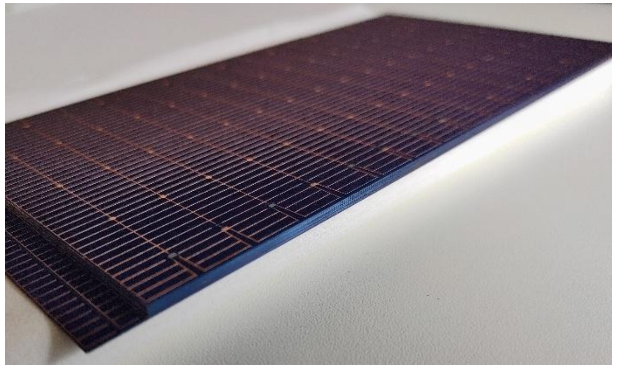
ITO 50 nm



ITO 50 nm
+ dielectric
+ copper

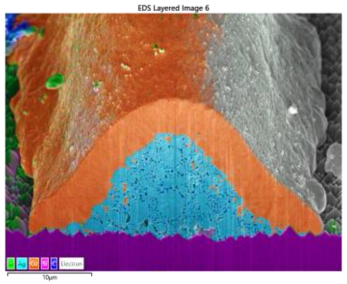
Thickness of dielectric layer adjusted for optimum ARC

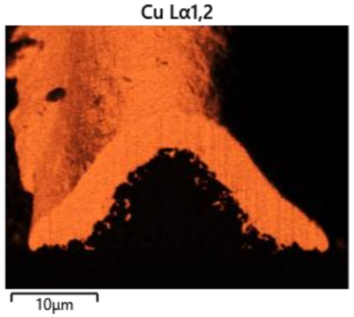
Cell edges are covered by the dielectric layer and well protected against parasitic plating.

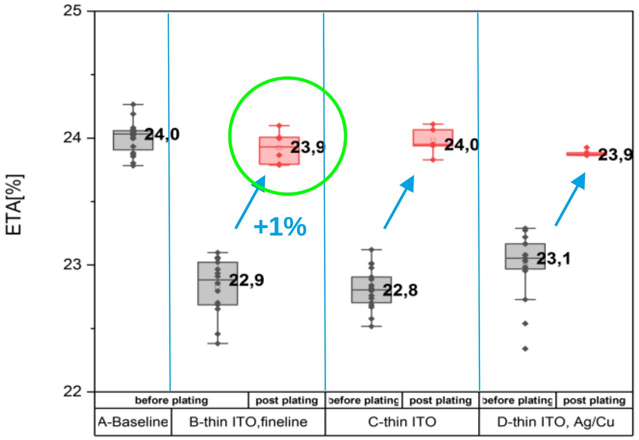


PLATED CELLS w. 50 nm ITO (1/2 M10)

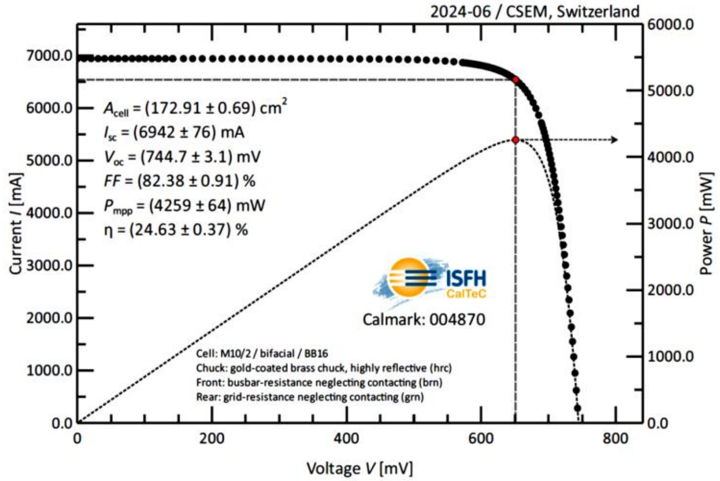
- Cells w. Ag or Ag-Cu paste seed grid





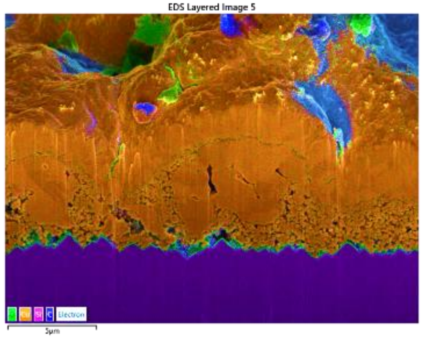


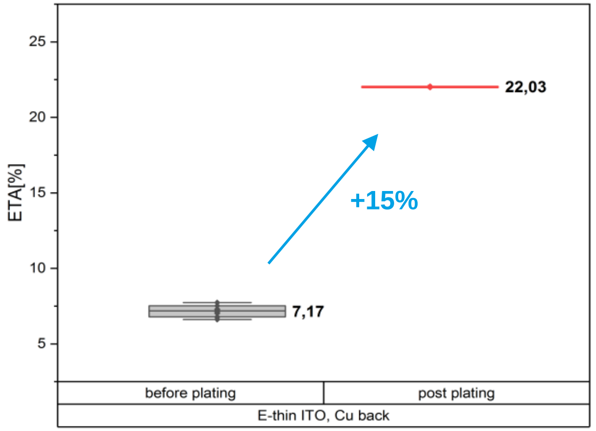
Internal IV measurement

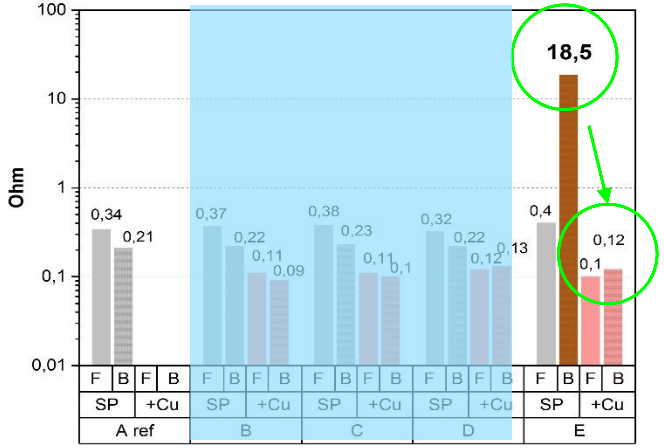


- Cells w. Cu plated on **PURE Cu paste**

Wide fingers from screen printing of this Cu paste – used only on the back. High line resistance **18.5 Ohm** (B2B).







Line resistance busbar to busbar.
Grey: as printed, red: w. plated Cu;
front & back

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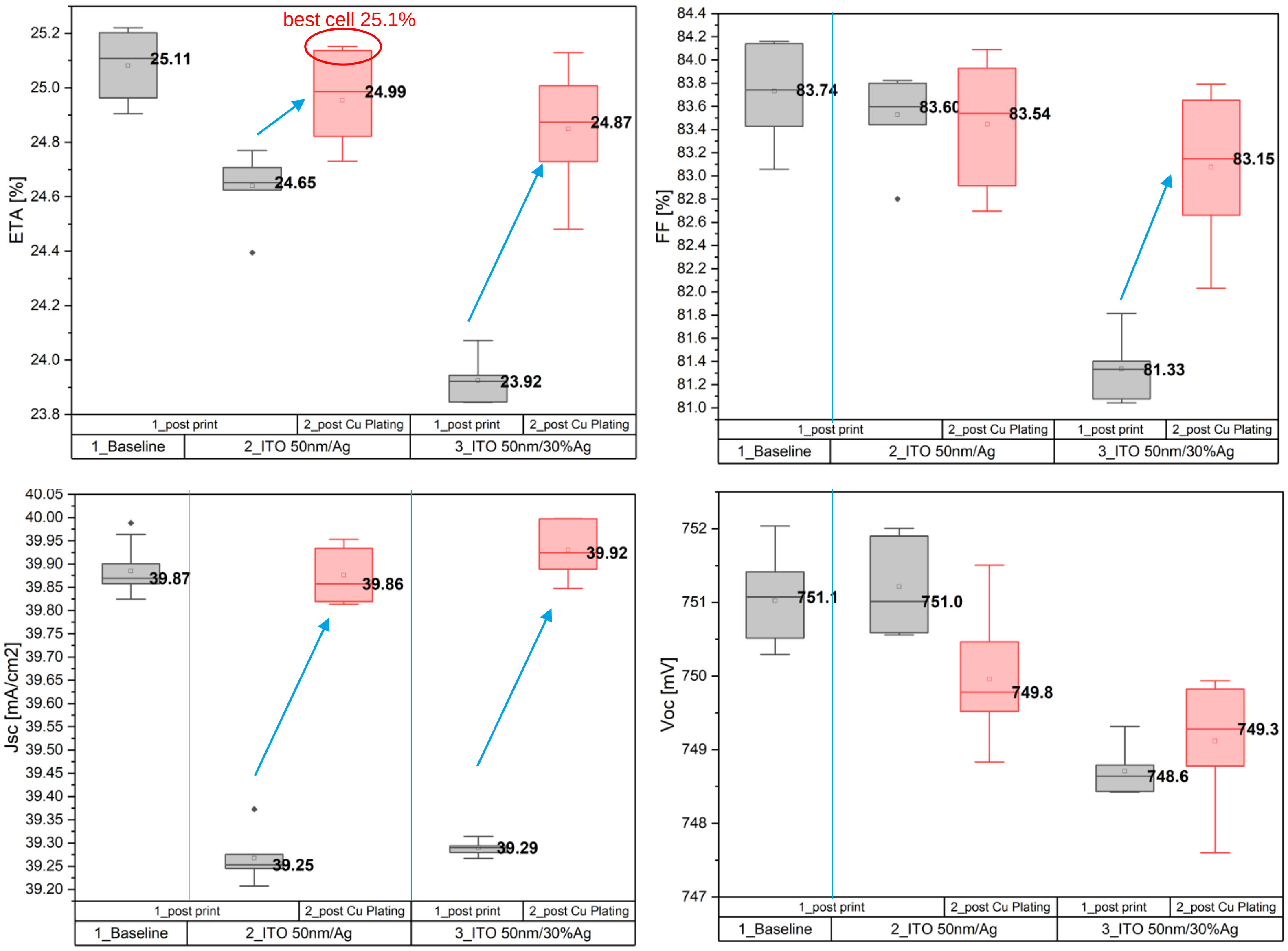
½ G12 w. 50 nm ITO

-Customer Sampling B

Group	ITO f [nm]	ITO r[nm]	Paste f	Paste r
1_Baseline	100	100	Ag	Ag
2_ITO 50nm/Ag	50	100	Ag	Ag
3_ITO 50nm/ 30% AgCu	50	100	Ag 30%	Ag 30%

- Plating results confirmed on half-G12 precursors from another manufacturer
- Same efficiency of best plated cells as of the reference group with full ITO and Ag-print (stencil)
- IV measurement from the precursor manufacturer



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½ G12 w. 30 nm ITO & M2 w. 15 nm ITO

-Customer Sampling C

- Precursors provided by a HJT cell manufacturer, with **30 nm ITO** (on the front) and Ag paste

Group	Voc [V]	Jsc [mA/cm²]	FF [%]	Eff. [%]
Travel reference, full ITO	0.744	39.1	83.1	24.12
30 nm ITO + dielectric + Cu	0.747	38.1	84.2	23.92

IV measurement by precursor manufacturer

- Efficiency after plating very close to the value of reference cells with full ITO
  Improvement through dielectric layer + copper plating: 1.4%abs.
- Jsc on precursors as received (w. 30 nm ITO) very low, to optimize.

- M2 precursors with **15 nm ITO** prepared by CEA INES: slightly lower efficiency of plated cells than of SP reference [1]
  - Is such a thin ITO layer still sufficient as barrier against copper?

1 A. Lanterne et al., Copper-Plating Metallization of low-Indium Heterjunction Solar Cells, MIW, 2024, https://miworkshop.info/wp-content/uploads/2024/11/B_02_Lanterne_MIW2024_poster-2024.pdf

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CELLS w. 15 nm ITO & PLATED COPPER: DH STABILITY

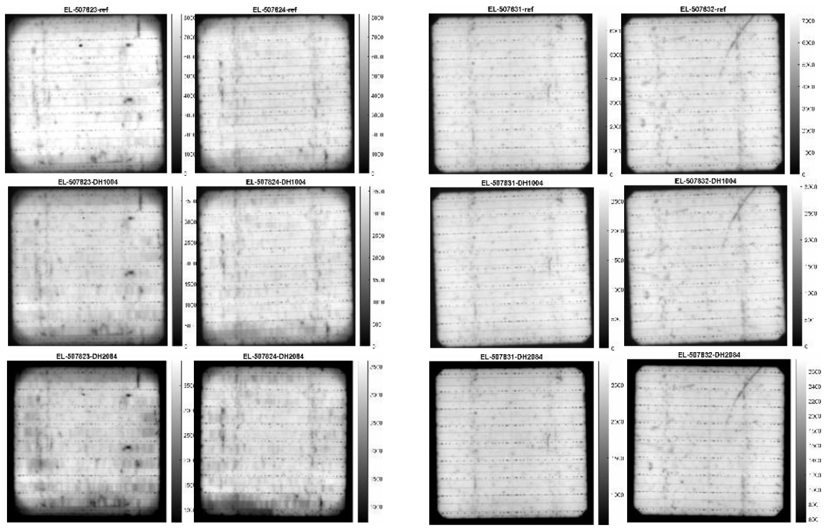
- Screen-printed reference:
  degradation in FF / interconnection
- Plated cells w. 15 nm ITO:
  degradation -2% after 2000 hours DH
  Voc stable!

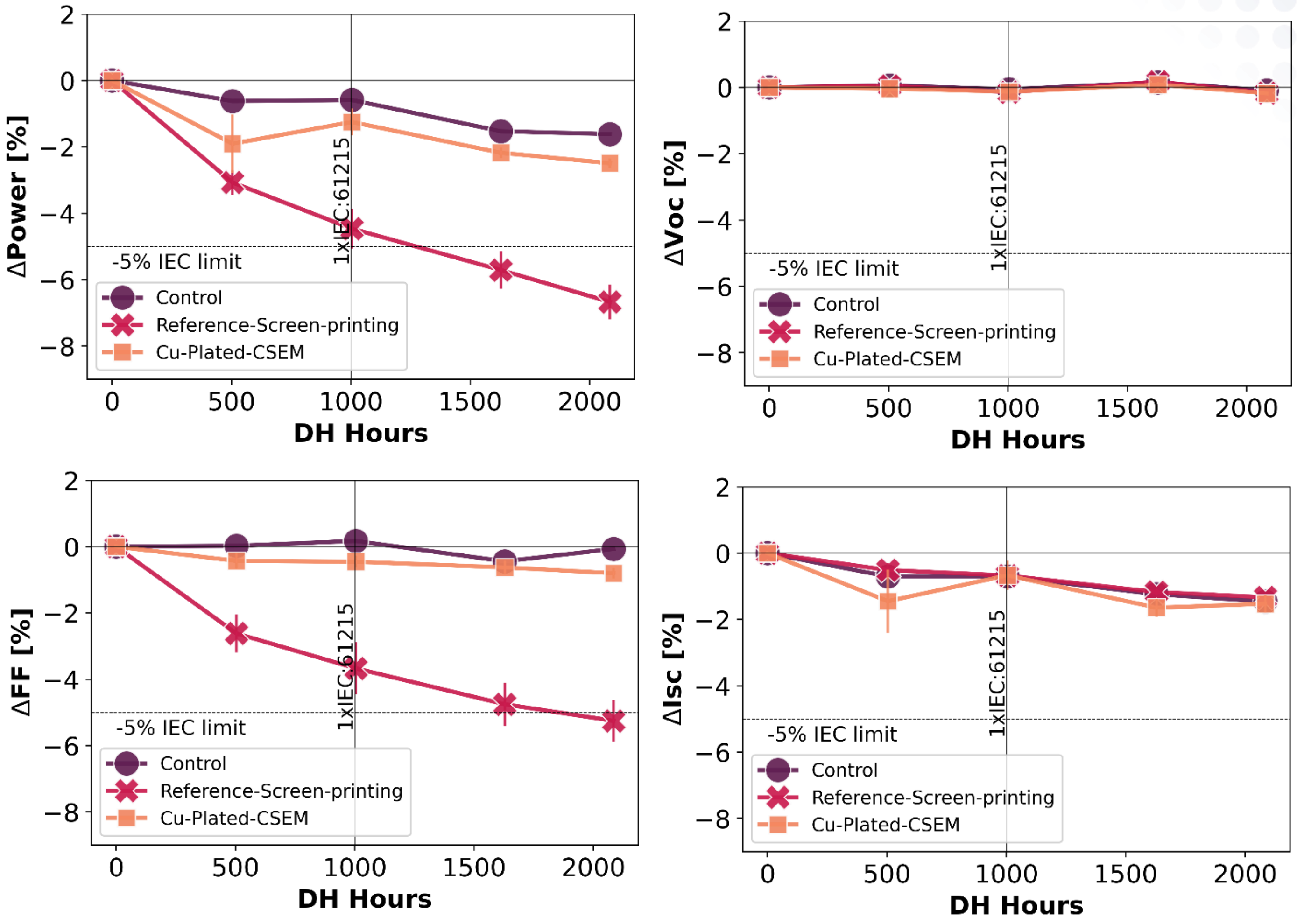
SP REFERENCE
100 nm ITO
Ag paste

15 nm ITO / SCC paste
+ DIELECTRIC LAYER
+ PLATED COPPER

1000 h

2000 h





M2 cells from CEA Ines, Smartwire interconnection at CSEM

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COST CALCULATION

- All data for cost calculation received from a multi-GW Chinese manufacturer; 2024
- Silver price = 1670 USD/kg
- Indium price = 357 USD/kg

Kept constant for all options:

- Efficiency 25.0%
- Power 5.52 W (½G12)
- Layout w. 18 busbars

Item / option	SCREEN PRINTING	PLATING Option 1	PLATING Option 2
SP fingers: Paste	**Cu/Ag-50%**	**Cu/Ag-30%**	**Cu/Ag-30%**
SP fingers: Laydown	**100%**	**60%**	**60%**
SP BB: Paste	100% Ag	Cu/Ag-30%	Cu/Ag-30%
SP BB: Laydown	100%	60%	60%
ITO FRONT	**100 nm**	**30 nm**	**30 nm**
ITO Back	**100 nm**	**80 nm**	**indium-free**
Equipment SP and PVD	baseline	baseline	baseline

Further savings through equipment modifications not considered in the calculation:
- Fingers and busbar print in one step
- Smaller PVD line for thinner ITO

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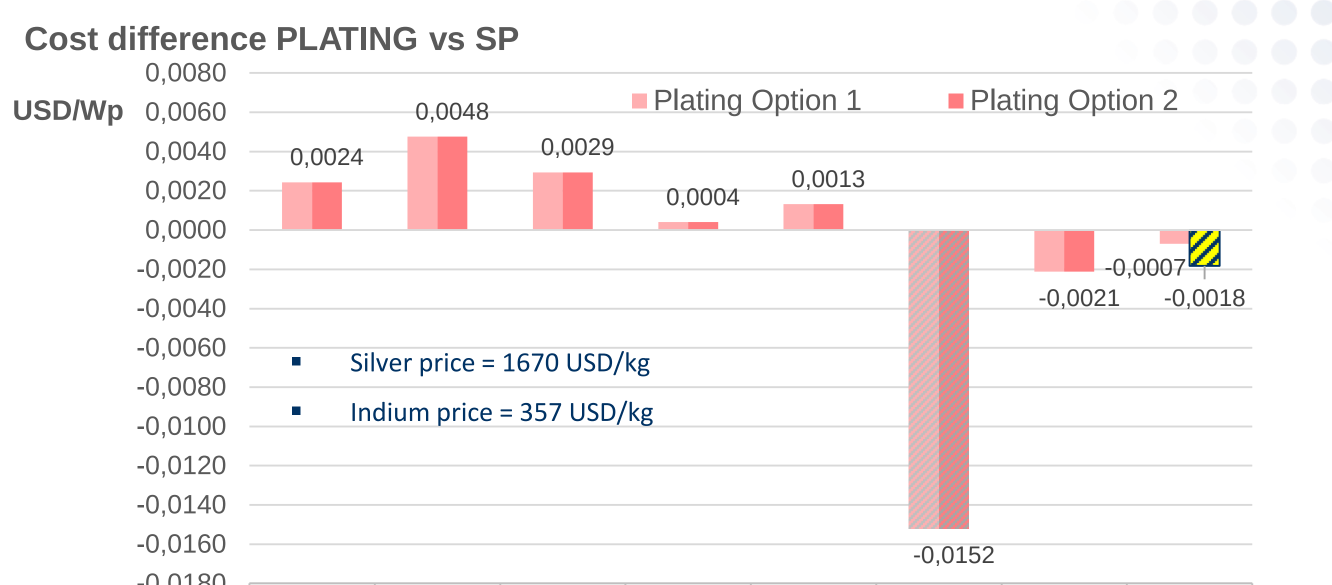
COST PLATING vs SP

- **Cost difference** for plating options 1 and 2 compared to baseline screen printing with silver-coated-copper paste (Cu/Ag-50%)
- Main additional costs for plating
  - PECVD and plating line
  - Chemicals and gases
- Savings: mainly silver paste, smaller impact of ITO reduction (at current In price)



	Deprec. PECVD + Plating	Chemi-cals & gases	Electri-city	Labor	Other manuf. cost	Silver cost	Indium FRONT	Indium back
Plating Option 1	0,0024	0,0048	0,0029	0,0004	0,0013	-0,0152	-0,0021	-0,0007
Plating Option 2	0,0024	0,0048	0,0029	0,0004	0,0013	-0,0152	-0,0021	-0,0018

- Overall, the process cost for plating is slightly lower than that of screen printing with silver-coated copper paste.
- **The consumption of silver as well as of indium is strongly reduced.**

Item / option	SCREEN PRINTING	PLATING Option 1	PLATING Option 2
CoO in USD/Wp (w/o Si)	0.051 (0.048 in Sep)	0.044 (0.044 in Sep)	0.043 (0.042 in Sep)
Ag reduction	100%	60%	60%
Indium on the cell in mg/Wp	4.7	2.6	0.7

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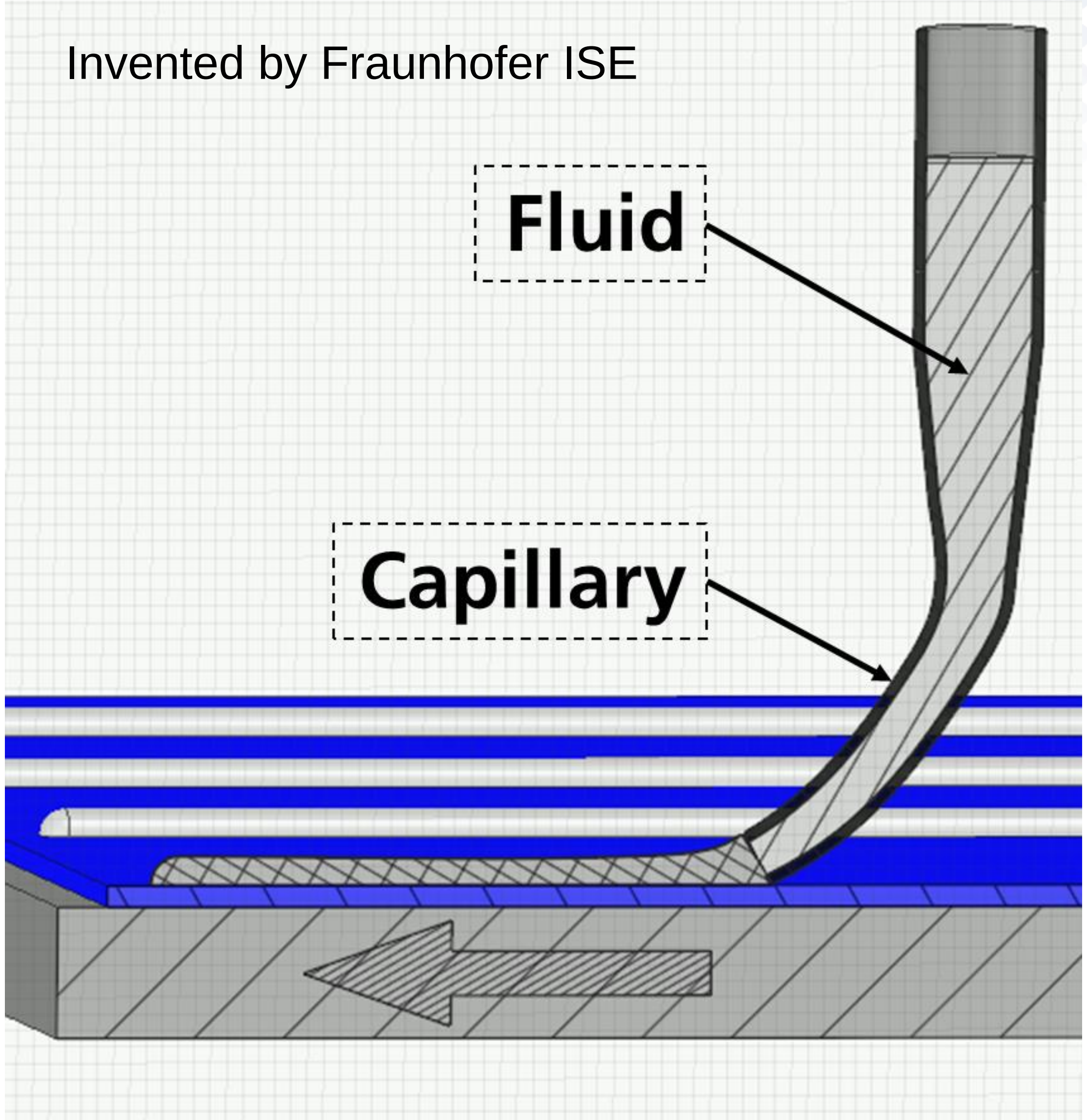
FLEXTRAIL PRINTING PRINCIPLE[1,2]

Working principle

- Flexible capillary in contact with substrate
  > Single-capillary printing so far
- Continuous printing
- Surface energies as driving forces
  > Independent printing technique
- Printing speed of up to 500 mm/s demonstrated

Motivation

- Wide viscosity range > little requirements for fluid
- Resource saving
- Broad field of applications



[1] M. Jahn, EP 3 736 050 (2022).
[2] J. Schube et al., *Energy Technology* (2022).

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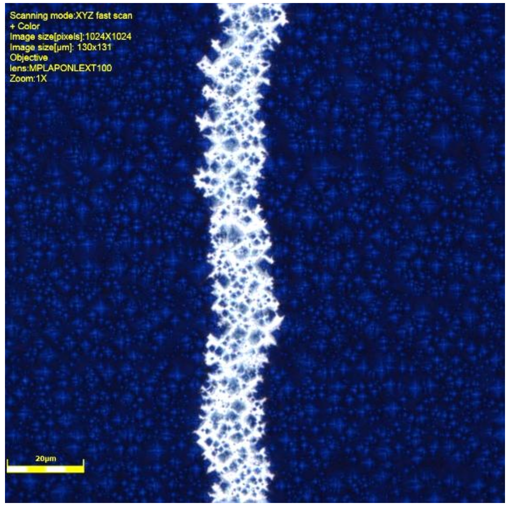
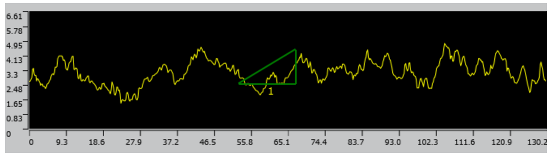
FLEXTRAIL PRINTING: FIRST TEST ON M2 PRECURSORS

- First test / print only on the front. Very shallow, even not fully continuous lines.
- Good copper coverage on this “almost-nothing”-seed-grid
- And:
  good adhesion of plated lines
  (tape test)

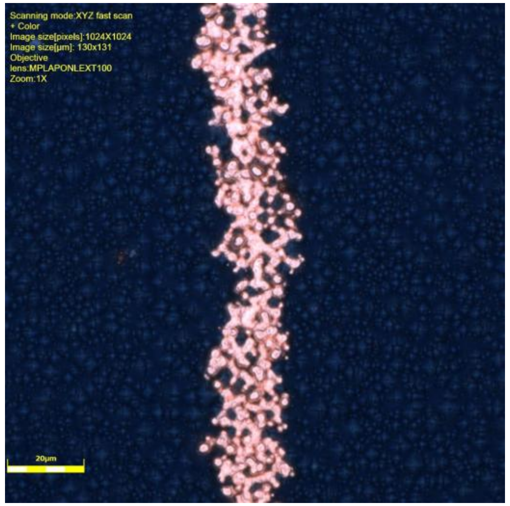
As printed



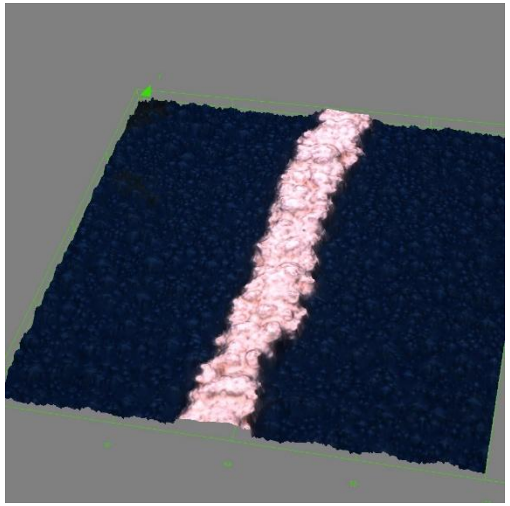


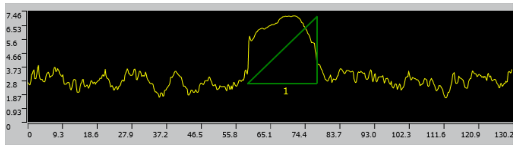
Width[µm]	Height[µm]
14.323	n.a.

Initial copper deposition



Plated line

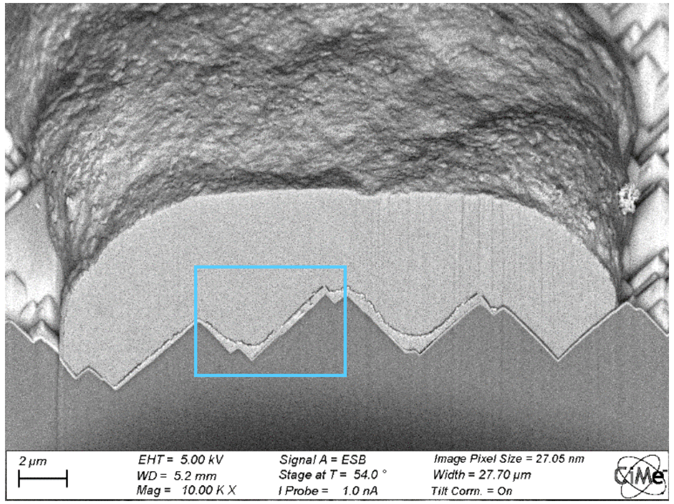


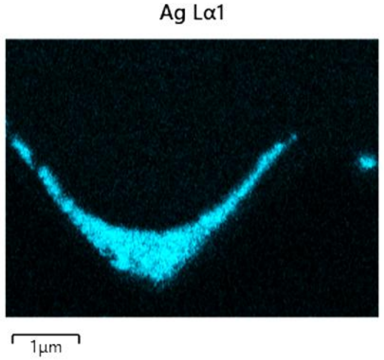


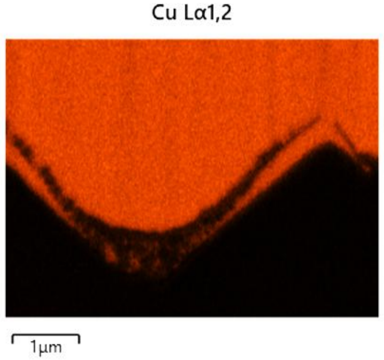
Width[µm]	Height[µm]
18.736	4.542

FLEXTRAIL PRINTING: FIRST TEST / CROSS SECTIONS

- Slight accumulation of the ink in the valleys of the pyramids Ink amount estimated to be below 1 mg/W.
- Copper signal observed also in between ink particles and in direct contact to ITO.

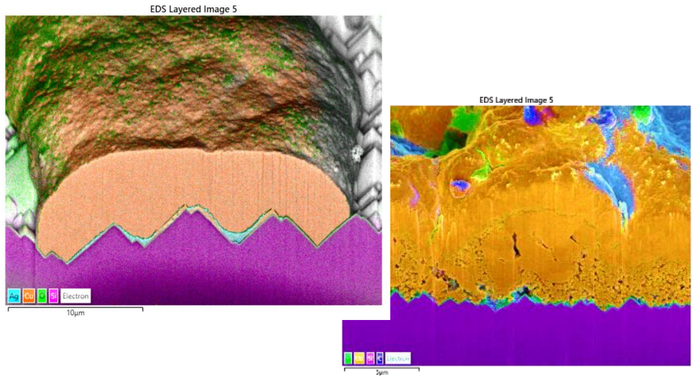






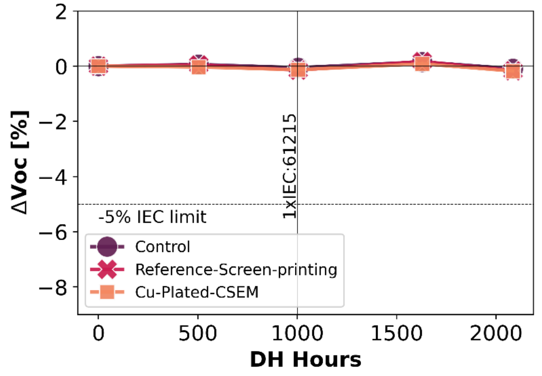
ENABLING SUSTAINABLE PRODUCTION OF HETEROJUNCTION CELLS:

- **Ag** **< 1mg/W**



Seed grid formation by **Flextrail** printing or with **pure copper paste**

- **In** **~ 0.7 mg/W**



15 nm ITO sufficient as copper barrier;
ARC: ITO+dielectric

THANK YOU VERY MUCH FOR YOUR ATTENTION!

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the European Union

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FACING THE CHALLENGES OF OUR TIME